Dual Channel Interleaved Synchronous-Rectified Buck Controller

General Description

The uP3861P is a compact dual-channel synchronous rectified buck controller specifically designed to operate with single 12V supply voltage and to deliver high quality output voltage for high power application. The two channels are operated with 180 degree phase interleaved. The two-channel output voltage has power on sequence set. It adopts external compensated voltage mode control to tightly regulate the feedback voltage to internal 1V reference voltage. The switching frequency is programmable from 50KHz to 400KHz, providing an optimal level of integrating to reduce size and const of the power supply.

The uP3861P integrates MOSFET drives that supply 12V+12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count.

Other features include under voltage lockout (UVLO), under voltage protection ,over voltage protection (OVP) and user programmable over temperature protection (OTP). With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions. This part is available in SOP-20L package.

Applications

- **ATX Power Supplies**
- **Power Supplies for Microprocessors or Subsystem Power Supplies**
- **Cable Modems, Set Top Boxes, and xDSL Modems**
- **Industrial Power Supplies; General Purpose Supplies**
- **5V or 12V Input DC-DC Regulators**
- **Low Voltage Distributed Power Supplies**

Ordering Information

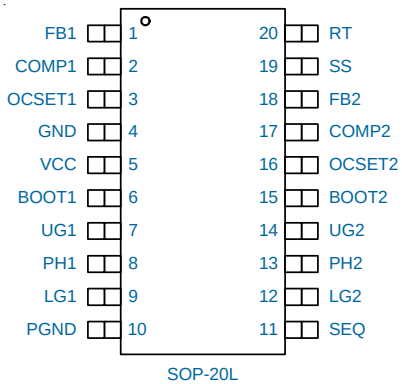
Order Number	Package	Top Marking
uP3861PSAF	SOP-20L	uP3861P

Note: uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

Features

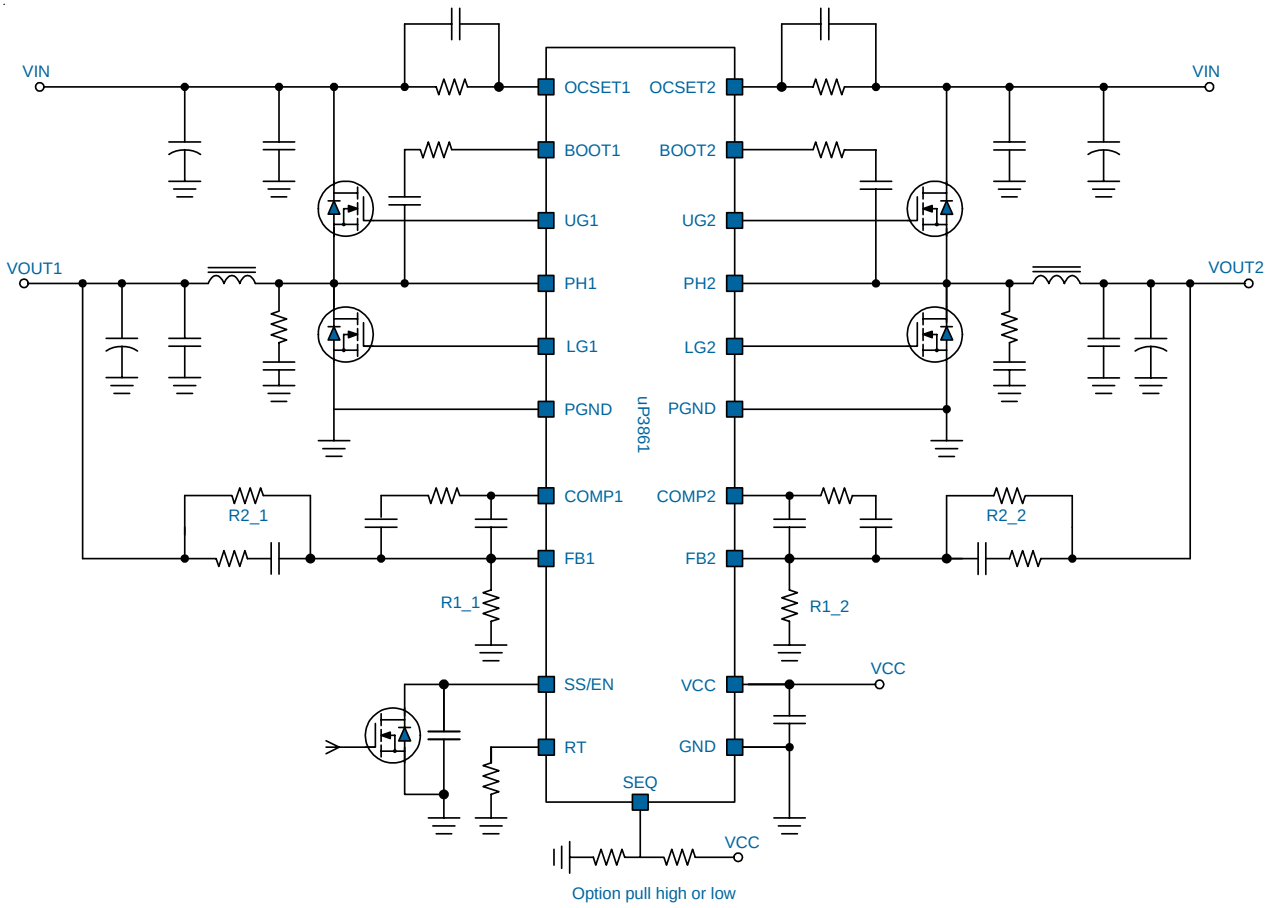
- **Dual Channel Synchronous Buck PWM Controller**
- **Operates Single with 12V Supply Voltage**
- **Wide Output Voltage Range 1V +/- 0.8%**
- **High-Side MOSFET's $R_{DS(ON)}$ Sensing**
- **Programmable Frequency Range from 50 kHz to 400kHz**
- **Voltage-Mode PWM Control**
- **0% to 90% Duty Cycle**
- **Shutdown and Soft-start Function**
- **UVP Specification is Implemented at 50% of VREF**
- **OVP Specification is Implemented at 120% of VREF**
- **Soft-Start**
- **Both Channels with 180 Degree Phase shift**
- **Integrated Boot Diode**
- **Over-Temperature Protection**
- **Sequence ON/OFF Controller**
- **SOP-20L Package**
- **RoHS Compliant and Halogen Free**

Pin Configuration



SOP-20L

Typical Application Circuit



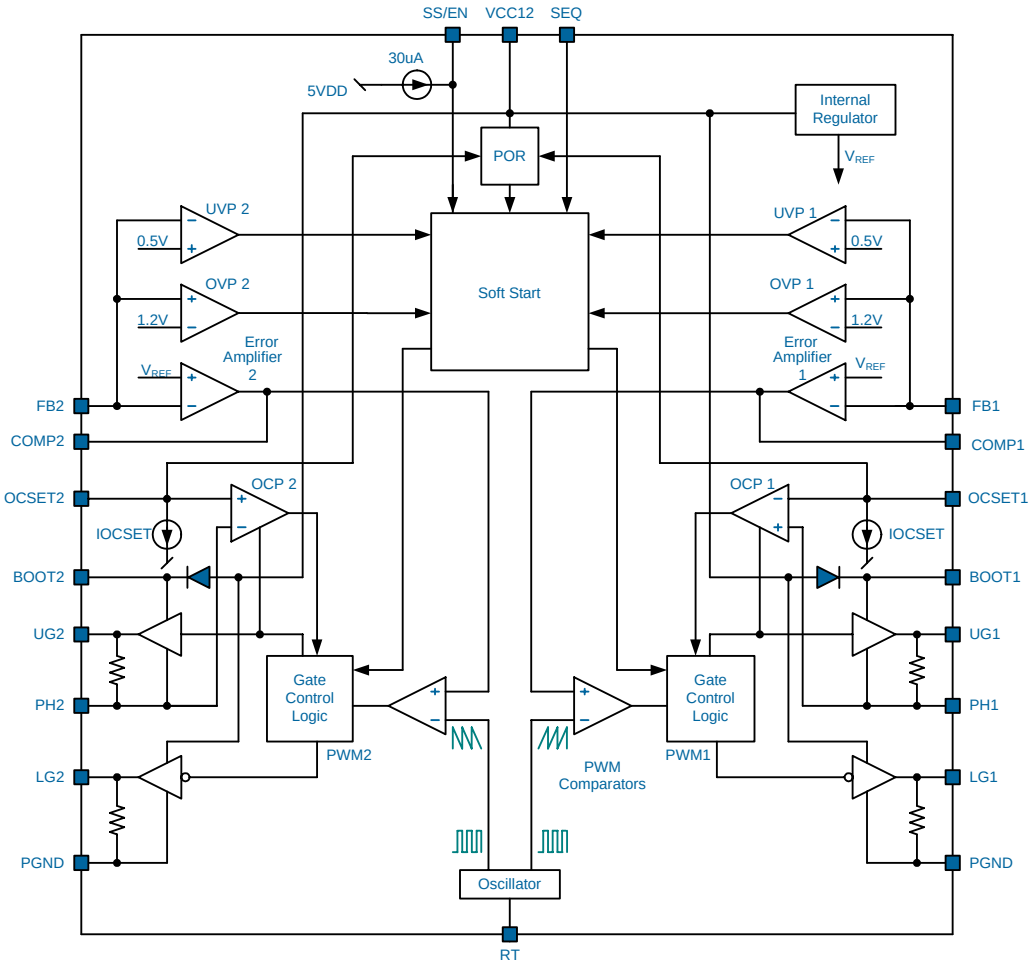
Functional Pin Description

Name	Pin Function
FB1	**Output Voltage Feedback 1 input.** The pin is the inverting input of the error amplifier 1. Connect a voltage divider to set the output voltage .
COMP1	**Compensation1 Output.** This pin is the output of the error amplifier 1 and the non-inverting input of PWM1 comparators. Connect a RC network to FB1 pin to compensate the voltage-control feedback loop of the channel1 converter.
OCSET1	**OCP1 Level Setting.** Connect a resistor to supply input of power stage to set the channel 1 over current protection threshold level. A capacitor in parallel with the resistor to filter out the switching noise
GND	**Analog Ground.**
VCC	**Supply Voltage for Control circuit.** This pin provides supply voltage for internal control circuit. The supply voltage is internally regulated to 5VDD for internal control circuit and VREF 1V. connect a well-decoupled 10.8V to 13.2V supply voltage to this pin. Ensure that decoupling capacitor is placed near the IC.
BOOT1	**Bootstrap 1 Supply for The Upper Gate Driver.** Connect the bootstrap capacitor C_{BOOT} between BOOT1 and PH1 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET 1.
UG1	**Upper Gate Driver 1 Output.** Connect this pin to the gate of upper MOSFET 1. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET 1 has turned off.
PH1	**PHASE1 Switch Node.** Connect this pin to the source the upper MOSFET 1 and the drain of the lower MOSFET 1. This pin is used as the sink for the UG1 drive and is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET1 has turned off.
LG1	**Lower Gate Driver output.** Connect this pin to the gate of lower MOSFET 1. Tie This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET 1 had turn off.
PGND	**Power Ground for The IC.** This pin is the return of the lower gate driver. Tie this pin the source of lower MOSFET with wide and short trace.
SEQ	**Power on Sequence.** The pin is self-biased low to select channel 1 soft-start first. If connect the pin to VCC , channel 2 will soft-start first.
LG2	**Lower Gate Driver Output.** Connect this pin to the gate of lower MOSFET 2. Tie This pin is monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET 2 had turn off.
PH2	**PHASE2 Switch Node.** Connect this pin to the source the upper MOSFET 2 and the drain of the lower MOSFET 2. This pin is used as the sink for the UG2 drive and is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET2 has turned off.
UG2	**Upper Gate Driver 2 Output.** Connect this pin to the gate of upper MOSFET 2. This pin is monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET 2 has turned off.
BOOT2	**Bootstrap 2 Supply for The Upper Gate Driver.** Connect the bootstrap capacitor C_{BOOT} between BOOT2 and PH2 pin to form a bootstrap circuit. The bootstrap capacitor provides the charge to turn on the upper MOSFET 2.
OCSET2	**OCP2 Level Setting.** Connect a resistor to supply input of power stage to set the channel 2 over current protection threshold level. A capacitor in parallel with the resistor to filter out the switching noise
COMP2	**Compensation 2 Output.** This pin is the output of the error amplifier 2 and the non-inverting input of PWM2 comparators. Connect a RC network to FB2 pin to compensate the voltage-control feedback loop of the channel 2 converter.

Functional Pin Description

Name	Pin Function
FB2	**Output Voltage Feedback 2 Input.** The pin is the inverting input of the error amplifier 2 . connect a voltage divider to set the output voltage .
SS/ Shut Down	**Soft Start Setting/Shut Down .** Connect a capacitor from this pin to GND to set the ramp-up slew of output voltage .when V_{SS} pulls below 0.7V shuts down the IC.
RT	**Frequency Setting Input.** Connect a resistor from this pin to GND to set switch frequency.

Functional Block Diagram



Functional Description

The uP3861P is a compact dual-channel synchronous-rectified buck controller specifically designed to operate with single 12V supply voltage and to deliver high quality output voltage. The two channels are operated with 180 degree phase shift and The two-channel output voltage has power on sequence set. It adopts external compensated voltage mode control to tightly regulate the feedback voltage to internal 1V. The switching frequency is programmable from 50KHz to 400KHz, providing an optimal level of integration to reduce size and cost of the power supply.

The uP3861P integrates MOSFET drives that support 12V+12V bootstrapped voltage for high efficiency power conversion. The bootstrap diode is built-in to simplify the circuit design and minimize external part count.

Other features include under-voltage protection and over-voltage protection. With aforementioned functions, this part provides customers a compact, high efficiency, well-protected and cost-effective solutions.

Supply Voltage

The VCC pin receives supply input to power the control circuit and a gate drive. This pin requires a minimum 1uF ceramic capacitor for locally bypassing. The bypassing capacitor should be placed physically near this pin.

An internal linear regulator regulates VCC supply voltage into a 5.0V voltage for internal control logic circuit and a 1V reference voltage

Power-on-Reset (POR)

The uP3861P continuously monitors 1.)VCC pin voltage, 2)OCSET1/2 pin voltage for power on reset. When the voltage on VCC and OCSET 1/2 exceeds their rising POR threshold voltage respectively (9.5V and 1.6V), the POR function initiates soft-start operation. Where the voltage at OCSET1/OCSET2 pin is equal to VIN1/VIN2 minus a fixed voltage drop (VOCSET1/VOCSET2=VIN1/VIN2-VROCSET1/VROCSET2).For operation with a single +12V power source, VIN1/VIN2 and VCC are equivalent and the +12V power source must exceed the rising VCC threshold. With all input supplies above their POR thresholds. The device initiates a soft-start interval.

Soft-Start/EN

The SS Pin controls the soft-start and enables/disables the controller. Connect a soft-start capacitor from SS pin to GND to set soft-start interval. When VCC reaches its power-on-reset threshold (9.5V), a soft-start current source ISS(30uA),starts to charge the capacitor. When the VSS reaches the threshold about 1 V, the internal 1.0V reference starts to rise and follows the Vss; the error amplifier output (Vcomp) suddenly rises to 1.1V, which is the valley of the triangle wave of the oscillator, leads the VOUT1/VOUT2 to start up. The up3861P VFB1 and VFB2 have power on sequence set by SEQ pin. When SEQ pulled GND and than VFB2 will start up after Vss rise up to 1.4V Figure1 shows the soft-start interval. when SEQ pulled VCC and than VFB1 will tart up after Vss rise up to 1.4V Figure2 shows the soft-start interval..

Before POR is released the SS pin is internally pulled low to ground when POR is released, an internal 30uA current source starts to charge Css, resulting in a linearly ramping-up voltage Vss.

$$T_{SS} = T3 - T1 = T4 - T2 = \frac{C_{SS}}{I_{SS}} \times 1$$

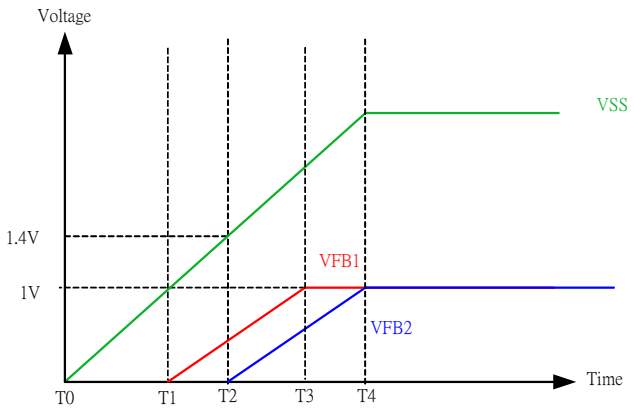


Figure 1. SEQ = GND, Soft-Start Sequence

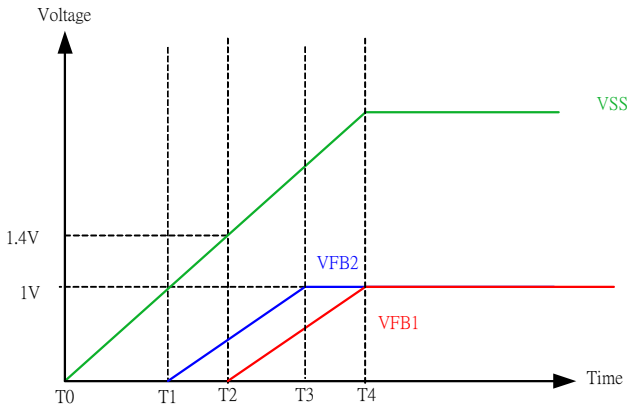


Figure 2. SEQ = Vcc, Soft-Start Sequence

Over Temperature protection (OTP)

The OTP is triggered and shuts down the uP3861P if the junction temperature is higher than 150°C. The OTP is a non-latch type protection. The uP3861P automatically initiates another soft start cycle if the junction temperature drops below 110°C.

Output Voltage Seting

The output voltage can be programmed by resistive divider connected to the FB1/2 pin as shown in the typical application circuit:

$$V_{OUT1/2} = 1.0V \times \frac{R1+R2}{R1}$$

Over Current protection (OCP)

The uP3861P monitors the voltage drop across the upper MOSFET for over-current protection (OCP). A resistor (R_{OCSET}) connected between OCSET pin and the drain of the upper MOSFET programs the OCP threshold level as show in figure 3. An internal 200uA current source flows through the $R_{OCSET1/2}$. Creating a voltage $V_{OCSET1/2}$ at OCSET as:

$$I_{OCSET1/2} = V_{IN} - 200uA \times R_{OCSET1/2}$$

The OCP comparator compares the VOCSET1/2 and VPHASE1/2 for over current protection when the upper MOSFET turn on if $V_{PH1/2}$ is lower than VOCSET1/2, an OCP is traiggered The OCP threshold level is given by:

$$I_{OCP1/2} = \frac{I_{OCSET1/2} \times R_{OCSET1/2}}{R_{DS(ON)}} = \frac{200uA \times R_{OCSET1/2}}{R_{DS(ON)}}$$

An OCP will shut down the device and discharge the Css with a 30uA sinking current source. When the Css is discharged completely, another soft start cycle is initiated.

If the over current condition is not removed during the soft start cycle, the uP3861P will shut down immediately when another OCP is triggered. However., the Vss keeps rising 30uA current source discharges the Css. If the over current condition is not removed, the re-soft-start cycle will repeat 3 times and then latch off uP3861P.

To avoid false trigger of OCP, variations of all parameters in above equation should be well considered, including:

1.) The $R_{DS(ON)}$ of MOSFET varies with temperature and the gate to source voltage. Consider the highest operation temperature and lowest gate to source voltage.

2.) Consider the minimum I_{OCSET}(~180uA) and minimum ROCSET.

3.) Consider the inductor ripple current.

4.) ROCSET is suggested to set above 1kΩ for the best stability.

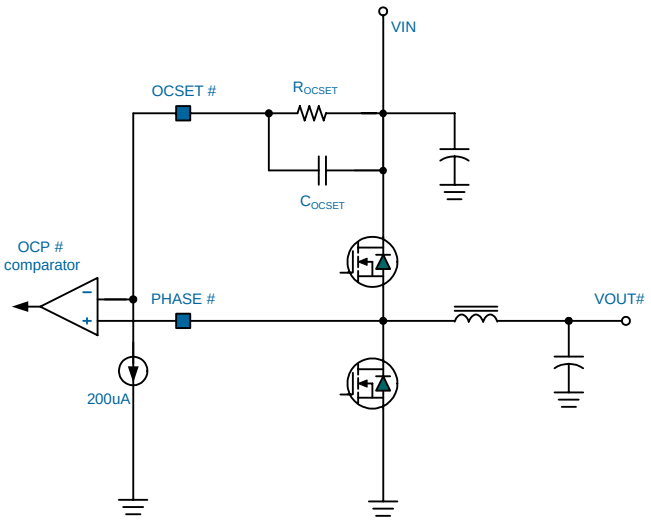


Figure 3. OCP Level Programming

Under Voltage Protection (UVP)

The FB1/2 voltage is monitored for under voltage protection after soft start end is asserted. If the FB1/2 voltage is lower than 0.5V (50% of 1V = 0.5V reference voltage), the UVP is triggered and shuts sown the uP3861P with about 3us time delay. The uP3861P turns off both upper and lower MOSFETs when UVP is triggered. The UVP is a latch-off type protection and can only be reset by POR of the device.

Over Voltage Protection (OVP)

The FB1/2 voltage is monitored for over voltage protection. If the FB1/2 voltage higher than 1.2V (120% of 1V =1.2V reference voltage), the OVP is triggered and shuts sown the uP3861P with about 10us time delay . The uP3861P turn off both upper and lower MOSFETs when OVP is triggered. The UVP is a latch-off type protection and can only be reset by POR of the device.

Oscillation Frequency programming

The uP3861P features adjustable switching frequency by a resistor connected to the RT pin. when the RT pin is floating. The uP3861P operates free-running 50KHz switch frequency. A resistor Rrt connected form RT pin to the ground programs the oscillation frequency as:

$$f_{OSC}(kHz) = 50 + \frac{7550}{R_{RT}(k\Omega)}$$

Figure 4 shows the relationship between oscillator frequency and R_{RT}.

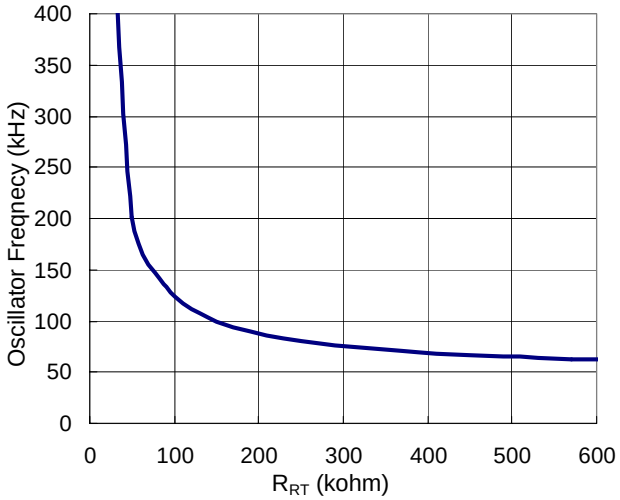


Figure 4. Oscillator Frequency vs. R_{RT}

Absolute Maximum Rating

Supply Input Voltage, $V_{CC,}$ PV_{CC} (Note1) ---------- -0.3V to +16V
BOOT to PH ---------- -0.3V to 16V
PH to GND
DC ---------- -0.3V to 16V
< 200ns ---------- -8V to 30V
BOOT to GND
DC ---------- -0.3V to (VCC + 16V)
< 200ns ---------- -5V to 42V
UG to PH
DC ---------- -0.3V to (BOOT-PH+0.3V)
< 200ns ---------- 5V to (BOOT-PH+0.3V)
LG to GND
DC ---------- -0.3V to (VCC+0.3V)
< 200ns ---------- 5V to (VCC+0.3V)
RT/OCSET ---------- VCC +0.3V
FB/COMP ---------- -0.3V to 7V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature Range ---------- -20°C to +150°C
Lead Temperature Range(Soldering 10sec) ---------- 260°C
ESD Rating (Note2)
HBM (Human Body Mode) ---------- 2kV
MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
SOP - 20L θ_{JA} ---------- 100°C/W
SOP - 20L θ_{JC} ---------- 30°C/W
Power Dissipation, P_D @ TA = 25°C
SOP - 20L ---------- 1.0W

Recommended Operation Conditions

Operating Junction Temperature Range (Note 4) ---------- -20°C to +125°C
Operating Ambient Temperature Range ---------- -20°C to +75°C
Supply Input Voltage, V_{CC} ---------- +10.8V to +13.2V
Converter Input Voltage, V_{IN} ---------- +2.2V to +13.2V
Converter Output Voltage, V_{OUT} ---------- +0.6V to + 5.0V
Converter Output Current, I_{OUT} ---------- +0A to + 30A

Electrical Characteristics

(V_{CC} = PV_{CC} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
Supply Voltage Range	V_{CC}		10.8	--	13.2	V
Supply Input Current	I_{CC}	UG and LG Open	--	5	10	mA
Power On Reset						
VCC POR Threshold	V_{CCRTH}	V_{CC} Rising.	9	9.5	10	V
VCC POR Threshold	V_{CCFTH_1}	V_{CC} Falling	7.5	8.0	8.5	V
Rising V_{OCSET} Threshold	V_{OCSET_TH}		--	1.6	--	V
V_{OCSET} Hysteresis Voltage	$V_{OCSETHYS}$		--	0.6	--	V
Oscillator						
Frequency Accuracy			-15	--	+15	%
Free Running Frequency	Fosc	RT = Open	--	50	--	kHz
Adjustment Range			50	--	400	kHz
Ramp Amplitude	Vosc		--	1.9	--	V
Minimum Duty Cycle			--	0	--	%
Duty Ration			0	--	90	%
Reference						
Reference Voltage	V_{REF}		--	1	--	V
Reference Voltage Tolerance			-0.8	--	+0.8	%
PWM Error Amplifier						
Open Loop Gain	Gain	R_L = 10K, C_L = 10pF	70	80	--	dB
Open Loop Bandwidth	GBWP	R_L = 10K, C_L = 10pF	--	10	--	MHz
Slew Rate	SR	R_L = 10K, C_L = 10pF	3	6	--	V/us
FB input current	$I_{FB1/2}$		--	0.01	0.1	uA
COMP High Voltage	V_{COMP_H}		--	5.5	--	V
COMP Low Voltage	V_{COMP_L}		--	0	--	V
COMP Source Current			--	2	--	mA
COMP Sink Current			--	2	--	mA
GATE Driver						
Upper Gate Source Impedance	R_{UG_SRC}	I_{UG} = 100mA sourcing	--	3	5	Ω
Upper Gate Sink Impedance	R_{UG_SNK}	I_{UG} = 100mA sinking	--	1	2	Ω
Lower Gate Source Impedance	R_{LG_SRC}	I_{LG} = 100mA sourcing	--	1.5	3.0	Ω
Lower Gate Sink Impedance	R_{LG_SNK}	I_{LG} = 100mA sinking	---	2	4	Ω
PH Falling to LG Rising Delay		V_{PH} < 1.2V to V_{LG} > 1.2V	--	30	--	ns
LG Falling to UG Rising Delay		V_{LG} < 1.2V to (V_{UG} - V_{PH}) > 1.2V	--	30	--	ns

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection						
Soft-start Charge Current	I_{SS}	V_{SS} = 0V	24	30	36	uA
OVP Threshold Level	V_{OVP}	VFB rising	--	1.3	--	V
OVP Delay Time			--	25	--	us
UVP Threshold Level	V_{UVP}	V_{FB} falling	--	0.55	--	V
UVP Delay Time			--	2	--	us
OTP level			--	150	--	^{0}C
OCSET Sink Current Source	$I_{OCSET1/2}$	$V_{OCSET1/2}$ = V_{CC} - 0.3	180	200	220	uA
OCSET Delay Time			--	3	--	us
SEQ						
Input High	SEQH		2.6	--	--	V
Input Low	SEQL		--	--	0.4	V
SEQ Pull Low Resistance			--	100	--	kΩ

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

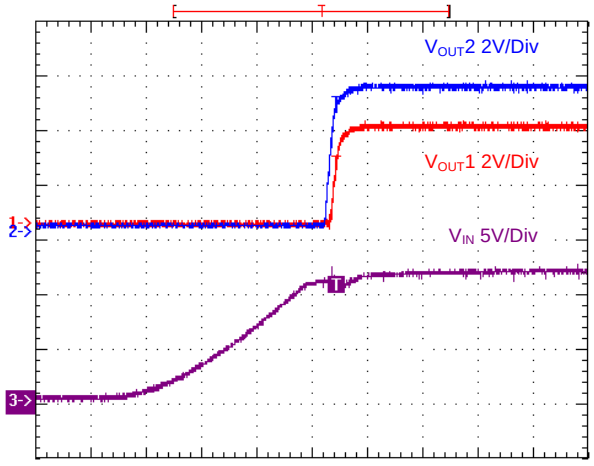
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25^{o}C on a low effective thermal conductivity test board of JEDEC 51-7 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

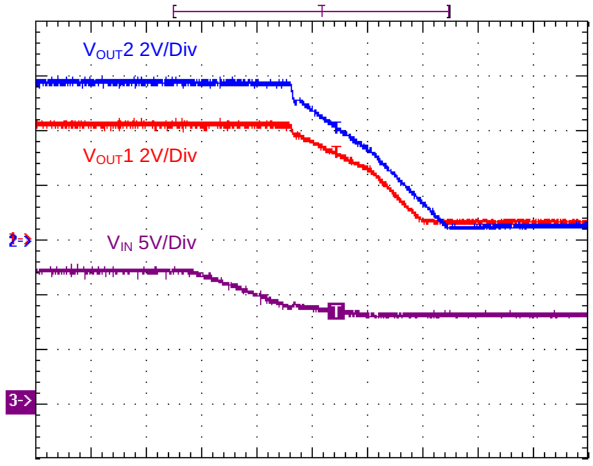
Typical Operation Characteristics

Power On Waveforms



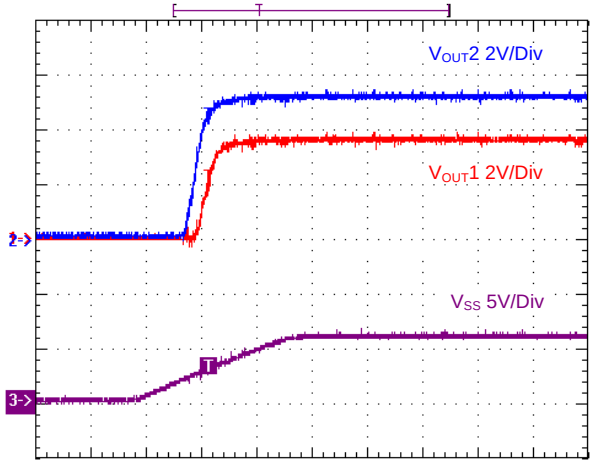
Time (4ms/Div)
V_{IN} = 12V, V_{CC} = 12V, I_{LOAD} = 2A

Power Off Waveforms



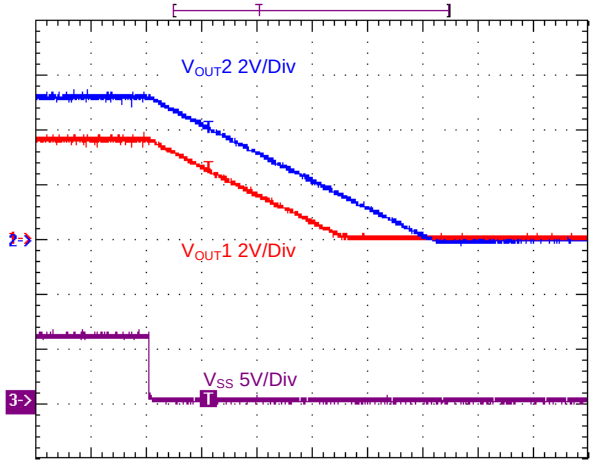
Time (4ms/Div)
V_{IN} = 12V, V_{CC} = 12V, I_{LOAD} = 2A

Enable for uP3861



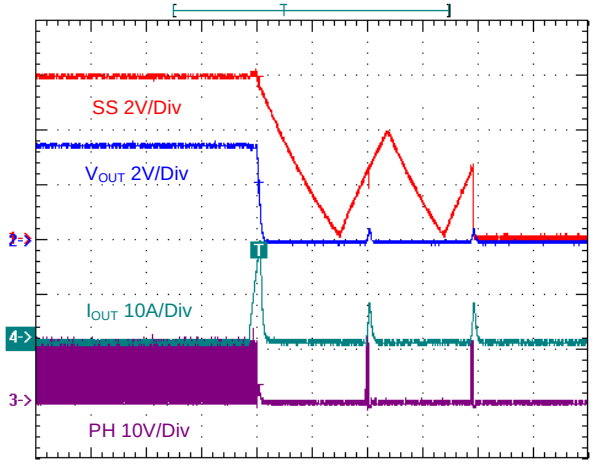
Time (2ms/Div)
V_{IN} = 12V, V_{CC} = 12V, I_{LOAD} = 2A

Disable for uP3861



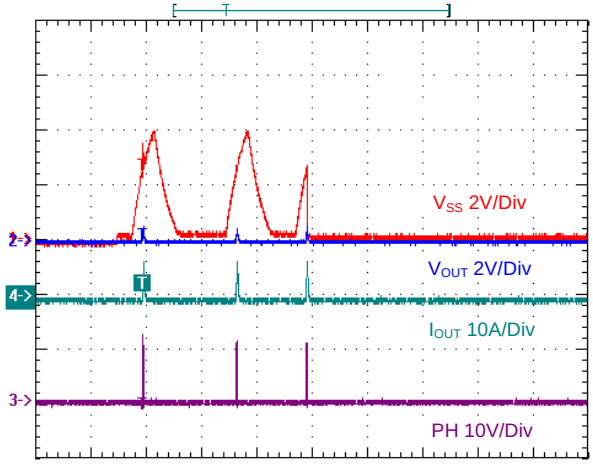
Time (2ms/Div)
V_{IN} = 12V, V_{CC} = 12V, I_{LOAD} = 2A

OCP



Time (4ms/Div)

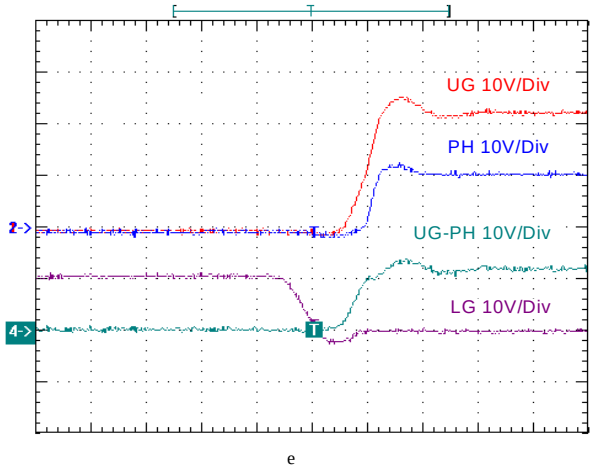
SCP



Time (10ms/Div)

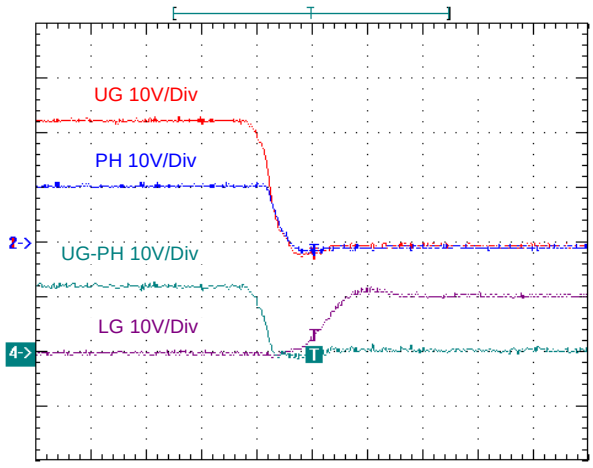
Typical Operation Characteristics

Gate Waveforms



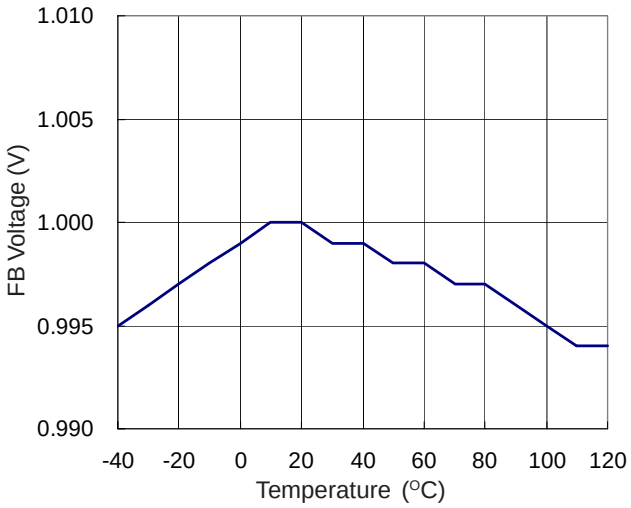
Time (40ns/Div)
V_{IN} = 12V, V_{CC} = 12V, I_{LOAD} = 10A

Gate Waveforms

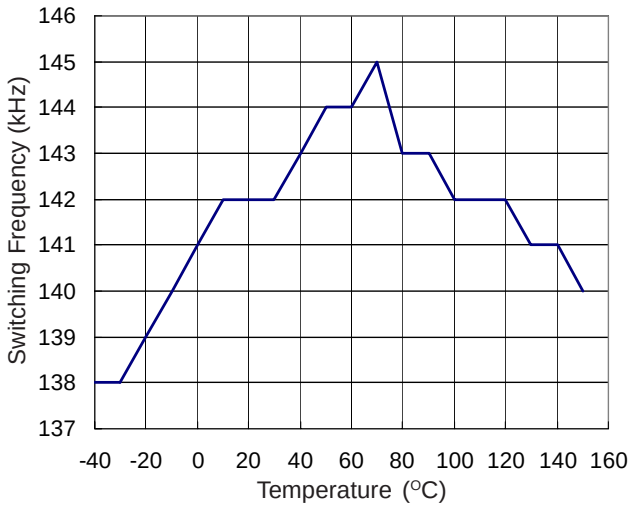


Time (40ns/Div)
V_{IN} = 12V, V_{CC} = 12V, I_{LOAD} = 10A

FB Voltage vs. Temperature



Switching Frequency vs. Temperature



Application Information

Power MOSFET Selection

External component selection is primarily determined by the maximum load current and begins with the selection of power MOSFET switches. The uP3861P requires two external N-channel power MOSFETs for upper (controlled) and lower (synchronous) switches. Important parameters for the power MOSFETs are the breakdown voltage $V_{(BR)DSS}$, on-resistance $R_{DS(ON)}$, reverse transfer capacitance C_{RSS}, maximum current $I_{DS(MAX)}$, gate supply requirements, and thermal management requirements.

The gate drive voltage is powered by VCC pin that receives 10.8V~13.2V supply voltage. When operating with a 12V power supply for VCC (or down to a minimum supply voltage of 8V), a wide variety of NMOSFETs can be used. Logic-level threshold MOSFET should be used if the input voltage is expected to drop below 8V. Since the lower MOSFET is used as the current sensing element, particular attention must be paid to its on-resistance. Look for $R_{DS(ON)}$ ratings at lowest gate driving voltage.

Special cautions should be exercised on the lower switch exhibiting very low threshold voltage $V_{GS(TH)}$. The shoot-through protection present aboard the uP3861P may be circumvented by these MOSFETs if they have large parasitic impedances and/or capacitances that would inhibit the gate of the MOSFET from being discharged below its threshold level before the complementary MOSFET is turned on. Also avoid MOSFETs with excessive switching times; the circuitry is expecting transitions to occur in under 50 nsec or so.

In high-current applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. The conduction losses are the largest component of power dissipation for both the upper and the lower MOSFETs. These losses are distributed between the two MOSFETs according to duty cycle. Since the uP3861P is operating in continuous conduction mode, the duty cycles for the MOSFETs are:

$$D_{UP} = \frac{V_{OUT}}{V_{IN}} \quad ; \quad D_{LO} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The resulting power dissipation in the MOSFETs at maximum output current are:

$$P_{UP} = I_{OUT}^2 \times R_{DS(ON)} \times D_{UP} + 0.5 \times I_{OUT} \times V_{IN} \times T_{SW} \times f_{OSC}$$

$$P_{LO} = I_{OUT}^2 \times R_{DS(ON)} \times D_{LO}$$

where T_{SW} is the combined switch ON and OFF time.

Both MOSFETs have I^2R losses and the top MOSFET includes an additional term for switching losses, which are largest at high input voltages. The bottom MOSFET losses are greatest when the bottom duty cycle is near 88%, during a short-circuit or at high input voltage. These equations assume linear voltage current transitions and do not adequately model power loss due the reverse-recovery of the lower MOSFET's body diode. Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

The gate-charge losses are dissipated by the uP3861P and don'theat the MOSFETs. However, large gate charge increases the switching interval, T_{SW} that increases the MOSFET switching losses. The gate-charge losses are calculated as:

$$P_G = V_{CC} \times (V_{CC} \times (C_{ISS\_UP} + C_{ISS\_LO}) + V_{IN} \times C_{RSS}) \times f_{OSC}$$

where C_{ISS_UP} is the input capacitance of the upper MOSFET, C_{ISS_LO} is the input capacitance of the lower MOSFET, and C_{RSS_UP} is the reverse transfer capacitance of the upper MOSFET. Make sure that the gate-charge loss will not cause over temperature at uP3861, especially with large gate capacitance and high supply voltage.

Output Inductor Selection

Output inductor selection usually is based the considerations of inductance, rated current, size requirement, and DC resistance (DC)

Given the desired input and output voltages, the inductor value and operating frequency determine the ripple current:

$$\Delta I_L = \frac{1}{f_{OSC} \times L_{OUT}} \times V_{OUT} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Highest efficiency operation is obtained at low frequency with small ripple current. However, achieving this requires a large inductor. There is a tradeoff between component size, efficiency and operating frequency. A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$.

There is another tradeoff between output ripple current/ voltage and response time to a transient load. Increasing the value of inductance reduces the output ripple current and voltage. However, the large inductance values reduce the converter's response time to a load transient.

Application Information

Maximum current ratings of the inductor are generally specified in two methods: permissible DC current and saturation current. Permissible DC current is the allowable DC current that causes 40^{O}C temperature raise. The saturation current is the allowable current that causes 10% inductance loss. Make sure that the inductor will not saturate over the operation conditions including temperature range, input voltage range, and maximum output current.

The size requirements refer to the area and height requirement for a particular design. For better efficiency, choose a low DC resistance inductor. DCR is usually inversely proportional to size.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs. size requirements and any radiated field/EMI requirements.

Input Capacitor Selection

The synchronous-rectified buck converter draws pulsed current with sharp edges from the input capacitor resulting in ripples and spikes at the input supply voltage. Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high frequency decoupling and bulk capacitors to supply the current needed each time upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of upper MOSET and the source of lower MOSFET to avoid the stray inductance along the connection trace.

The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline. The RMS current rating requirement for the input capacitor of a buck converter is calculated as:

$$I_{IN(RMS)} = I_{OUT(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{IN(RMS)} = I_{OUT(RMS)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

For a through-hole design, several electrolytic capacitors may be needed. For surface mount designs, solid tantalum capacitors can also be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Output Capacitor Selection

An output capacitor is required to filter the output and supply the load transient current. The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \le \Delta I_L \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}}\right)$$

Since ΔIL increases with input voltage, the output ripple is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating. Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types.

The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout. Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (Effective Series Resistance) and voltage rating requirements rather than actual capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage

and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes.

However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading.

Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Bootstrap Capacitor Selection

An external bootstrap capacitor C_{BOOT} connected to the BOOT pin supplies the gate drive voltage for the upper MOSFET. This capacitor is charged through the internal diode when the PHASE node is low. When the upper MOSFET turns on, the PHASE node rises to V_{IN} and the BOOT pin rises to approximately V_{IN} + V_{CC}. The boot capacitor needs to store about 100 times the gate charge required by the upper MOSFET. In most applications 0.1uF to 0.47uF, X5R or X7R dielectric capacitor is adequate.

PCB Layout Considerations

High speed switching and relatively large peak currents in a synchronous-rectified buck converter make the PCB layout a very important part of design. Fast current switching from one device to another in a synchronous-rectified buck converter causes voltage spikes across the interconnecting impedances and parasitic circuit elements. The voltage spikes can degrade efficiency and radiate noise that result in overvoltage stress on devices. Careful component placement layout and printed circuit design minimizes the voltage spikes induced in the converter.

Follow the layout guidelines for optimal performance of uP3861

1 The upper and lower MOSFETs turn on/off and conduct pulsed current alternatively with high slew rate transition. Any inductance in the switched current path generates a large voltage spike during the switching. The interconnecting wires indicated by red heavy lines conduct pulsed current with sharp transient and should be part of a ground or power plane in a printed circuit board to minimize the voltage spike. Make all the connection the top layer with wide, copper filled areas.

2 Place the power components as physically close as possible.

2.1 Place the input capacitors, especially the high-frequency ceramic decoupling capacitors, directly to the drain of upper MOSFET ad the source of the lower MOSFET. To reduce the ESR replace the single input capacitor with two parallel units

2.2 Place the output capacitor between the converter and load.

3 Place the uP3861P near the upper and lower MOSFETs with pins 6 to 9 or 12 to 15 facing the power components. Keep the components connected to pins 1 to 5 or 17 to 20 close to the uP3861P and away from the inductor and other noise sources (noise sensitive components).

4 Use a dedicated grounding plane and use vias to ground all critical components to this layer. The ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs. Use an immediate via to connect the components to ground plane including GND of uP3861P Use several bigger vias for power components.

5 Apply another solid layer as a power plane and cut this plane into smaller islands of common voltage levels. The power plane should support the input power and output power nodes to maintain good voltage filtering and to keep power losses low. Also, for higher currents, it is recommended to use a multilayer board to help with heat sinking power components.

6 The PHASE node is subject to very high dV/dt voltages. Stray capacitance between this island and the surrounding circuitry tend to induce current spike and capacitive noise coupling. Keep the sensitive circuit away from the PHASE node and keep the PCB area small to limit the capacitive coupling. However, the PCB area should be kept moderate since it also acts as main heat convection path of the lower MOSFET.

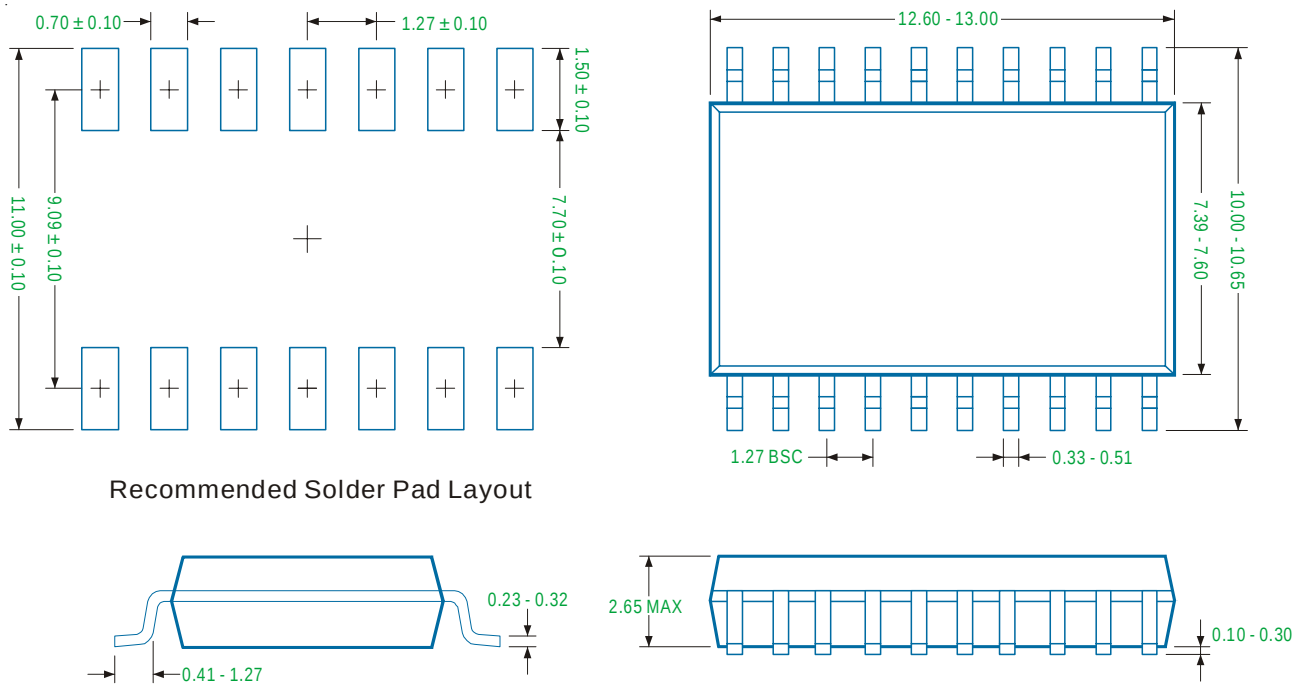
7 uP3861P sources/sinks impulse current with 2A peak to turn on/off the upper and lower MOSFETs. The connecting trance between the controller and gate/source of the MOSFET should be wide and short to minimize the parasitic inductance along the traces.

8 Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power component.

9 Provide local VCC decoupling between VCC and GND pins. Locate the capacitor, C_{BOOT} as close as practical to the BOOT and PHASE pins.

Package Information

SOP-20L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shell not exceed 0.15mm.

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